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PATENT APPLICATION

ATTORNEY DOCKET NO. 10971308-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): John G. McBride

Confirmation No.:

Application No.: 09/273,784

Examiner: Phan, T.

Filing Date: March 22, 1999

Group Art Unit: 2123

Title: Method and Apparatus for Evaluating the Quality of Network Nodes

COMMISSIONER FOR PATENTS
Washington, D.C. 20231

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith in **triplicate** is the Appeal Brief in this application with respect to the Notice of Appeal filed on **July 26, 2002**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $320.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$110.00
( )	two months	$400.00
( )	three months	$920.00
( )	four months	$1440.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$320.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Respectfully submitted,

John G. McBride

By Daniel R. McClure

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:	)	
	)	
John G. McBride	)	Group Art Unit: 2123
	)	
Serial No.: 09/273,784	)	Examiner: Phan, T.
	)	
Filed: March 22, 1999	)	HP Docket No. 10971308-1
	)	TKHR Dkt. No. 50814-1470
	)	
For: METHOD AND APPARATUS FOR EVALUATING THE QUALITY OF NETWORK NODES	)	

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents Box: Appeal Brief, Washington, D.C. 20231 on Aug 8, 2002.

H. Chin Barnhill

Signature – Hui Chin Barnhill

APPEAL BRIEF UNDER 37 C.F.R. §1.192

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

This is an appeal from the decision of Examiner Thai Phan, Group Art Unit 2123, of April 24, 2002 (Paper No. 7), rejecting claims 1-20 in the present application and making the rejection FINAL.

I. REAL PARTY IN INTEREST

The real party in interest of the instant application is Hewlett-Packard Company, a Delaware corporation, having its principal place of business in Palo Alto, California.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claims 1-20 are pending in the application. The FINAL Office Action mailed April 24, 2002, rejected all claims 1-20. Specifically, claims 15-20 were rejected under 35 U.S.C. § 101. Claims 1-20 were rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent 5,446,674 to Ikeda et al. For the reasons set further herein, Applicants respectfully request that these rejections be overturned.

IV. STATUS OF AMENDMENTS

No amendments have been submitted after the FINAL Office Action, and all amendments submit prior to that have been entered.

V. SUMMARY OF THE INVENTION

The present invention provides a method and apparatus for evaluating a gate of an integrated circuit to determine whether or not the gate has acceptable immunity to noise. The apparatus comprises a computer configured to execute a rules checker program 100 which receives input relating to characteristics of a static gate 138 (or 163) contained in the integrated circuit. The gate 138 comprises at least two field effect transistors (FETs). Each FET has a width and the characteristics received in the input to the rules checker program 100 include the widths of the field effect transistors. The rules checker program 100 analyzes the widths of the FETs to determine whether or not the gate has an acceptable noise immunity.

Each gate typically comprises a plurality of FETs 139, 141, 142, 143, usually an NFET 142, 143 and a PFET 139, 141, and input terminals A, B for receiving input signals. The rules checker program 100 processes the widths of the PFETs 139, 141 and NFETs 142, 143 to obtain at least a first numerical value relating to the widths. The rules checker program 100 utilizes the first numerical value to access one or more threshold noise level values from a memory device in communication with the computer. The rules checker program determines noise levels on the inputs A, B, either through calculation or simulation. The rules checker program 100 compares the determined noise levels with the threshold values and uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

VI. CONCISE STATEMENT OF THE ISSUES PRESENTED FOR REVIEW

The issues in this appeal are: (1) whether claims 15-20 are unpatentable under 35 U.S.C. §101; and (2) whether claims 1-20 are unpatentable under 35 U.S.C. 102(b) over U.S. Patent 5,446,674 to Ikeda et al.

VII. GROUPING OF THE CLAIMS

The claims can generally be divided into ten (10) claim groupings, as set out below. For purposes of the argument set forth in this appeal brief, one claim from each group will be evaluated and discussed in connection with the prior art. The claim groups include:

(1) Claim Group I, which comprises claims 1, 7, 8, and 14;

(2) Claim Group II, which comprises claims 2 and 9;

(3) Claim Group III, which comprises claims 3 and 10;

(4) Claim Group IV, which comprises claims 4 and 11;

(5) Claim Group V, which comprises claims 5, 6, 12, and 13;

(6) Claim Group VI, which comprises claim 15;

(7) Claim Group VII, which comprises claim 16;

(8) Claim Group VIII, which comprises claim 17;

(9) Claim Group IX, which comprises claim 18; and

(10) Claim Group X, which comprises claims 19 and 20.

Reasons that Claim Groups Do Not Stand or Fall Together

Although, in reality, all claims of an application are distinct, Applicants have grouped the claims of the present application into ten distinct claim groups. One claim for each group has been chosen as the exemplary claim. The reason that the claims for any given group do not stand or fall with any claims of another group is, ultimately, because they are of differing scope. This differing scope is more specifically set out below.

In regard to Claim Group I, each of the claims 1, 7, 8, and 14 are directed to an apparatus for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise. The apparatus of claim 1 includes a rules checker program that analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity. Independent claim 1 is the representative claim of Claim Group I.

In regard to Claim Group II, each of the claims 2 and 9 further defines features of the gate of claim 1 (and 8). Should the Board determine that the narrowed features of the gate, as defined in claim 2 define this claim over the cited art reference, then claim 2 will stand or fall independently of the conclusion regarding claim 1.

In regard to Claim Group III, each of the claims 3 and 10 further defines features of the rules checker program of claim 2 (and 9). Should the Board determine that the narrowed

features of the rules checker program, as defined in claim 3 define this claim over the cited art reference, then claim 3 will stand or fall independently of the conclusion regarding the claims of Claim Groups I or II.

In regard to Claim Group IV, each of the claims 4 and 11 further defines features of the rules checker program of claim 3 (and 10). Should the Board determine that the narrowed features of the rules checker program, as defined in claim 4 define this claim over the cited art reference, then claim 4 will stand or fall independently of the conclusion regarding the claims of Claim Groups I, II or III.

In regard to Claim Group V, each of the claims 5, 6, 12, and 13 further defines features of the rules checker program of claim 4 (and 11). Should the Board determine that the narrowed features of the rules checker program, as defined in claim 5 define this claim over the cited art reference, then claim 5 will stand or fall independently of the conclusion regarding the claims of Claim Groups I, II, III, or IV.

In regard to Claim Groups VI through X, the claims in these claim groups loosely correspond to the claims of Claim Groups I through V, respectively. However, in addition to the substantive bases advanced by the Office Action for rejecting the claims of Claim Groups I through V, the Office Action also rejected the claims of Claim Groups VI through X under 35 U.S.C. § 101. Therefore, the claims of these claim groups could not be properly combined with the claims of Claim Groups I through V.

VIII. ARGUMENT

A. Fundamental Distinction of the Ikeda Patent

Applicant respectfully submits that the substantive rejections of claim 1-20 of the present application based upon Ikeda should be overturned, for reasons that will be

specifically discussed below. However, before addressing the details of the specific rejections, Applicant notes that there are fundamental differences between the system of Ikeda and the present invention. As summarized above, the present invention is directed to a method for evaluating a gate node to determine whether the gate node has been designed to have an acceptable level of noise immunity. The Ikeda patent only mentions the term "noise" in the context of crosstalk noise, and not in the manner taught and treated by the present invention.

In this regard, Ikeda recognizes that a transistor having low output impedance is prone to exert the influence of crosstalk on other wires. However, Ideka also recognizes that a transistor of high output impedance is susceptible to crosstalk from other wires. Accordingly, the system of the Ikeda patent is concerned with crosstalk verification. Furthermore, the system disclosed by Ikeda appears to reference wire patterns and the capacitance measurements therebetween to determine whether crosstalk noise will be problematic. These fundamental differences are embodied in the pending claims of the present application.

B. <u>Discussion of Claim Group I</u>

With regard to the claims of Claim Group I, the Office Action rejected claims 1, 7, 8, and 14 under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent 5,446,674 to Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

In rejecting claim 1, the Office Action stated:

> As per claims 1 and 15, Ikeda anticipated method and operation system for checking design rule as claimed. According to Ikeda, the method and system for design rule checker includes a computer configured to execute a rule checker program, wherein the design rule being checked for an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters

> such as width, length, connected in device channel, etc. ("Summary of the Invention", col. 1, line 44 to col. 2, line 24, col. 2, lines 24-53, col. 5, lines 18-56, col. 9, line 45 to col. 10, line 10). The program is designed to check transistor susceptible to noise in the cross-talk influence (col. 2, lines 7-24, col. 5, lines 18-56, col. 9, line 54-col 10, line 2), including checking noise susceptible or noise immunity as claimed for transistors to other transistors because they are parts of noise control scheme.

The undersigned has closely reviewed the Ikeda reference and submits that it does not disclose the invention as defined by the independent claim 1 of the present application.

Specifically, independent claim 1 recites:

> 1. An apparatus ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the apparatus comprising:
> a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, ***the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully submits that the rejection of claim 1 should be overturned for at least the reason that Ikeda fails to disclose or teach at least the features emphasized above.

As set forth above, Ikeda is directed to a crosstalk verification device. It operates by calculating the magnitude of ***crosstalk noise*** as a function of the wire-to-wire capacitance, in order to specify a portion in which the magnitude of crosstalk noise exceeds reference voltages (see e.g., col. 3, lines 46-60 and the Abstract of Ikeda).

In contrast, claim 1 specifies the analysis of widths of field effect transistors within a static gate, to determine whether the gate has an acceptable ***noise immunity***. Simply stated, Ikeda does not teach this claimed aspect, and therefore cannot form a proper anticipatory reference. Furthermore, the undersigned performed an electronic search of the entire text of

the Ikeda patent for the term "noise immunity" and this term is not mentioned anywhere within the Ikeda patent.

The Office Action cited col. 9, line 45 through col. 10, line 10 of Ikeda as allegedly teaching the claimed portion of the rules checker program that analyzes the widths of FETs to determine whether or not the gate has an acceptable level of noise immunity. In fact, this portion of Ikeda teaches the comparison of a width to length ratio (W/L) with a stored reference value to identify "the transistor prone to exert crosstalk influence and the transistor susceptible to crosstalk." (col. 9, line 68 through col. 10, line 1). In this respect, Ikeda teaches that a transistor with a low output impedance (W/L greater than first reference value) is prone to exert the influence of crosstalk, while a transistor of high output impedance (W/L less than second reference value) is susceptible to crosstalk. Again, and significantly, the assessment of the likelihood of exerting crosstalk or the susceptibility to crosstalk of the Ikeda patent is different than the assessment of noise immunity, as defined by claim 1 of the present application.

For at least the foregoing reasons, Applicant respectfully submits that the rejection of claim 1 (and 7, 8, and 14) is misplaced and should be overturned by the Board.

C. Discussion of Claim Group II

With regard to the claims of Claim Group II, the Office Action rejected claims 2 and 9 under 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

The Office Action rejected claim 2 stating only that:

> Ikeda anticipated reading transistor design parameters for design rule check as claimed. Such transistor circuit design would include for example inverter gate, p-channel and n-channel transistor, CMOS channel parameters, design parameters, etc. as well-known in transistor circuit design.

On its face, this rejection is legally deficient, because it fails to even allege all of the features that are defined in claim 2. In this regard, claim 2 recites:

> 2. The apparatus of claim 1, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, ***the rules checker program processing the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths, the rules checker program utilizing the first numerical value to access first and second threshold values stored in a memory device in communication with the computer***, the rules checker program determining noise levels on the inputs, the rules checker program comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

(*Emphasis added.*)

To constitute a proper anticipatory reference to claim 2, Ikeda must disclose every feature of claim 2. Ikeda fails to do this. More significantly, the Office Action has not even alleged that the features of claim 2 that have been emphasized above are disclosed in Ikeda. For this reason alone, the Examiner has failed to make a legally-proper, prima facie rejection of claim 2, and the Board should overturn the rejection. Furthermore, Applicant has reviewed the entirety of the Ikeda patent, and has failed to locate or identify any proper or legitimate disclosure of the elements emphasized above.

Accordingly, Applicant respectfully requests that the Board overturn the rejection of claim 2 (and 9).

D. <u>Discussion of Claim Group III</u>

With regard to the claims of Claim Group III, the Office Action rejected claims 3 and 10 under 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

The Office Action rejected claim 3 stating only that:

> As per claims 3-7, the rule checker program as in the art of record obtains transistor design parameters or extracting the design parameters as claimed, and checks with the operating conditions as claimed ("Summary of the Invention").

On its face, this rejection is legally deficient, because it fails to even allege all of the features that are defined in claim 3. In this regard, claim 3 recites:

> 3. The apparatus of claim 2, wherein ***the rules checker program generates a first model of the gate in order to process the widths of the P and N field effect transistors***, the first representation of the gate consisting of a single N field effect transistor and a single P field effect transistor, ***the rules checker program obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the rules checker program to access the first and second threshold values stored in the memory device***, wherein when the first and second inputs are high, ***the rules checker program determines noise levels on the first and second inputs and compares the determined noise levels to the first and second threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the first model***, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first model, the rules checker program determines that the gate has an acceptable immunity to noise.

(*Emphasis added.*)

To constitute a proper anticipatory reference to claim 3, Ikeda must disclose every feature of claim 3. Ikeda fails to do this. More significantly, the Office Action has not even alleged that the features of claim 3 that have been emphasized above are disclosed in Ikeda. For this reason alone, the Examiner has failed to make a legally-proper, prima facie rejection of claim 3, and the Board should overturn the rejection. Furthermore, Applicant has reviewed the entirety of the Ikeda patent, and has failed to locate or identify any proper or legitimate disclosure of the elements emphasized above.

Accordingly, Applicant respectfully requests that the Board overturn the rejection of claim 3 (and 10).

E. Discussion of Claim Group IV

With regard to the claims of Claim Group IV, the Office Action rejected claims 4 and 11 under 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

The Office Action rejected claim 4 stating only that:

> As per claims 3-7, the rule checker program as in the art of record obtains transistor design parameters or extracting the design parameters as claimed, and checks with the operating conditions as claimed ("Summary of the Invention").

On its face, this rejection is legally deficient, because it fails to even allege all of the features that are defined in claim 4. In this regard, claim 4 recites:

> 4. The apparatus of claim 3, wherein ***the rules checker program processes the widths of the P and N field effect transistors by generating a second model of the gate***, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, ***the rules checker program obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the rules checker program to access a third and fourth threshold values stored in the memory device***, wherein the rules checker program determines noise levels on the first and second inputs when the first and second inputs are low ***and compares the determined noise levels to the third and fourth threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model***, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the rules checker program determines that the gate has an acceptable noise immunity.

(*Emphasis added.*)

To constitute a proper anticipatory reference to claim 4, Ikeda must disclose every feature of claim 4. Ikeda fails to do this. More significantly, the Office Action has not even alleged that the features of claim 4 that have been emphasized above are disclosed in Ikeda. For example, claim 4 calls for the generation of a second model and the access of third and

forth threshold values, which are used to make the noise immunity determination. Simply state, Ikeda fails to disclose any of these features, nor does the Examiner make any specific allegations in this regard.

For this reason alone, the Examiner has failed to make a legally-proper, prima facie rejection of claim 4, and the Board should overturn the rejection. Furthermore, Applicant has reviewed the entirety of the Ikeda patent, and has failed to locate or identify any proper or legitimate disclosure of the elements emphasized above. Accordingly, Applicant respectfully requests that the Board overturn the rejection of claim 4 (and 11).

F. Discussion of Claim Group V

With regard to the claims of Claim Group V, the Office Action rejected claims 5, 6, 12 and 13 under 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

The Office Action rejected claim 5 stating only that:

> As per claims 3-7, the rule checker program as in the art of record obtains transistor design parameters or extracting the design parameters as claimed, and checks with the operating conditions as claimed ("Summary of the Invention").

On its face, this rejection is legally deficient, because it fails to even allege all of the features that are defined in claim 5. In this regard, claim 5 recites:

> 5. The apparatus of claim 4, wherein ***the rules checker program processes the widths of the P and N field effect transistors by generating a third model of the gate***, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, ***the rules checker program obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the rules checker program to access a fifth and sixth threshold values stored in the memory device***, wherein when the

> first input is high, the rules checker program determines the noise level on the first input and compares the determined noise level to the fifth threshold value, wherein when the first input is low, the rules checker program determines the noise level on the first input ***and compares the determined noise level to the sixth threshold value, wherein the results of the comparisons are used by the rules checker program to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model***, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the rules checker program determines that the gate has an acceptable noise immunity.

(*Emphasis added.*)

To constitute a proper anticipatory reference to claim 4, Ikeda must disclose every feature of claim 5. Ikeda fails to do this. More significantly, the Office Action has not even alleged that the features of claim 5 that have been emphasized above are disclosed in Ikeda. For example, claim 5 calls for the generation of a third model and the access of fifth and sixth threshold values, which are used to make the noise immunity determination. Simply stated, Ikeda fails to disclose any of these features, nor does the Examiner make any specific allegations in this regard.

For this reason alone, the Examiner has failed to make a legally-proper, prima facie rejection of claim 5, and the Board should overturn the rejection. Furthermore, Applicant has reviewed the entirety of the Ikeda patent, and has failed to locate or identify any proper or legitimate disclosure of the elements emphasized above. Accordingly, Applicant respectfully requests that the Board overturn the rejection of claim 5 (and 6, 12, and 13).

G. Discussion of Claim Group VI

With regard to the claim of Claim Group VI, the Office Action rejected claim 15 under both 35 U.S.C. § 101 as being directed to non-statutory subject matter and 35 U.S.C. §

102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

The Office Action rejected claim 15 under 35 U.S.C. § 101 alleging that "the claimed computer program ... is directed to a data structure [and] is necessarily to be converted into executable code and executed by a computer to meet statutory requirement." This rejection is just wrong, and is inconsistent with the prevailing case law as well as numerous other decisions made by the Patent Office. In this regard, the Federal Circuit has made clear that computer-readable media are legitimate statutory subject matter. Furthermore, the Patent Office Action has issued numerous patents with claims directed to "computer-readable mediums" set forth using the same language as Applicant has used for claim 15. The following is a list of just a few such patents (each issued on May 28, 2002):

U.S. Patent 6,397,381 (claim 1);
U.S. Patent 6,397,354 (claim 24);
U.S. Patent 6,397,352 (claim 14);
U.S. Patent 6,397,335 (claim 9);
U.S. Patent 6,397,208 (claim 7); and
U.S. Patent 6,397,169 (claim 7).

Therefore, as an administrative agency, which must act consistently from matter to matter and from applicant to applicant, the Patent Office must withdraw this rejection.

Furthermore, and more importantly, the rejection is misplaced and should be withdrawn. In this regard, Applicant respectfully submits that claim 15 is NOT directed to a data structure, but rather to a "computer-readable medium." In this regard, claim 15 recites:

> *15.* A ***computer-readable medium containing a rules checker computer program,*** the computer program evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:
>
> code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

As is clearly recited, the subject matter of claim 15 is directed to a computer-readable medium that "contains" a rules checker computer program. Therefore, claim 15 is properly directed to statutory subject matter (computer-readable media), and the rejection of claim 15 (as being directed to a data structure) is misplaced and should be overturned.

With regard to the substantive rejection of claim 15 (i.e., the rejection under 35 U.S.C. § 102(b) as anticipated by Ikeda), Applicant submits that the rejection of claim 15 should be overturned for the same reasons advanced above in connection with claim 1.

H. Discussion of Claim Group VII

With regard to the claim of Claim Group VII, the Office Action rejected claim 16 under both 35 U.S.C. § 101 as being directed to non-statutory subject matter and 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

With regard to the rejection under 35 U.S.C. § 101, Applicant respectfully submits that this rejection should be overturned for the same reason discussed above in connection with claim 15. With regard to the substantive rejection of claim 16 (i.e., the rejection under 35 U.S.C. § 102(b) as anticipated by Ikeda), Applicant submits that the rejection of claim 16 should be overturned for the same reasons advanced above in connection with claim 2.

Applicant has separated claim 16 into a separate claim group because it does not necessarily stand or fall with claim 2, due to the rejection under 35 U.S.C. § 101.

I. Discussion of Claim Group VIII

With regard to the claim of Claim Group VIII, the Office Action rejected claim 17 under both 35 U.S.C. § 101 as being directed to non-statutory subject matter and 35 U.S.C. §

102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

With regard to the rejection under 35 U.S.C. § 101, Applicant respectfully submits that this rejection should be overturned for the same reason discussed above in connection with claim 15. With regard to the substantive rejection of claim 17 (i.e., the rejection under 35 U.S.C. § 102(b) as anticipated by Ikeda), Applicant submits that the rejection of claim 17 should be overturned for the same reasons advanced above in connection with claim 3.

Applicant has separated claim 17 into a separate claim group because it does not necessarily stand or fall with claim 3, due to the rejection under 35 U.S.C. § 101.

J. Discussion of Claim Group IX

With regard to the claim of Claim Group IX, the Office Action rejected claim 18 under both 35 U.S.C. § 101 as being directed to non-statutory subject matter and 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

With regard to the rejection under 35 U.S.C. § 101, Applicant respectfully submits that this rejection should be overturned for the same reason discussed above in connection with claim 15. With regard to the substantive rejection of claim 18 (i.e., the rejection under 35 U.S.C. § 102(b) as anticipated by Ikeda), Applicant submits that the rejection of claim 18 should be overturned for the same reasons advanced above in connection with claim 4.

Applicant has separated claim 18 into a separate claim group because it does not necessarily stand or fall with claim 4, due to the rejection under 35 U.S.C. § 101.

K. Discussion of Claim Group X

With regard to the claims of Claim Group X, the Office Action rejected claims 19 and 20 under both 35 U.S.C. § 101 as being directed to non-statutory subject matter and 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

With regard to the rejection under 35 U.S.C. § 101, Applicant respectfully submits that this rejection should be overturned for the same reason discussed above in connection with claim 15. With regard to the substantive rejection of claim 19 (i.e., the rejection under 35 U.S.C. § 102(b) as anticipated by Ikeda), Applicant submits that the rejection of claim 10 should be overturned for the same reasons advanced above in connection with claim 5.

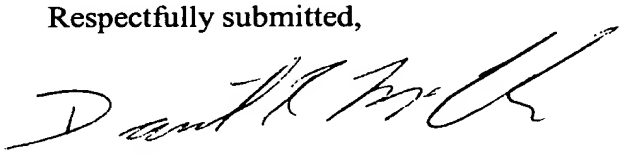
Applicant has separated claim 19 into a separate claim group because it does not necessarily stand or fall with claim 5, due to the rejection under 35 U.S.C. § 101.

IX. CONCLUSION

Based upon the foregoing discussion, Applicants respectfully requests that the Examiner's final rejection of claims 1-20 be overruled and withdrawn by the Board, and that the application be allowed to issue as a patent with all pending claims 1-20.

Please charge Hewlett-Packard Company's deposit account 08-2025 in the amount of $310 for the filing of this Appeal Brief. No additional fees are believed to be due in connection with this Appeal Brief. If, however, any additional fees are deemed to be payable, you are hereby authorized to charge any such fees to deposit account No. 08-2025.

Respectfully submitted,



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X. APPENDIX

Claims

1. An apparatus for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the apparatus comprising:

a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

2. The apparatus of claim 1, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the rules checker program processing the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths, the rules checker program utilizing the first numerical value to access first and second threshold values stored in a memory device in communication with the computer, the rules checker program determining noise levels on the inputs, the rules checker program comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

3. The apparatus of claim 2, wherein the rules checker program generates a first model of the gate in order to process the widths of the P and N field effect transistors, the first representation of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the rules checker program to access the first and second threshold values stored in the memory device, wherein when the first and second inputs are high, the rules checker program determines noise levels on the first and second inputs and compares the determined noise levels to the first and second threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the first model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first model, the rules checker program determines that the gate has an acceptable immunity to noise.

4. The apparatus of claim 3, wherein the rules checker program processes the widths of the P and N field effect transistors by generating a second model of the gate, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the rules checker program to access a third and fourth threshold values stored in the memory device, wherein the rules checker program determines noise levels on the first and second inputs when the first and second inputs are low and compares the

determined noise levels to the third and fourth threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the rules checker program determines that the gate has an acceptable noise immunity.

5. The apparatus of claim 4, wherein the rules checker program processes the widths of the P and N field effect transistors by generating a third model of the gate, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the rules checker program to access a fifth and sixth threshold values stored in the memory device, wherein when the first input is high, the rules checker program determines the noise level on the first input and compares the determined noise level to the fifth threshold value, wherein when the first input is low, the rules checker program determines the noise level on the first input and compares the determined noise level to the sixth threshold value, wherein the results of the comparisons are used by the rules checker program to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the rules checker program determines that the gate has an acceptable noise immunity.

6. The apparatus of claim 5, wherein the rules checker program processes the widths of the P and N field effect transistors by generating a fourth model of the gate, the fourth model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, the fourth ratio corresponding to a fourth numerical value, the fourth numerical value being used by the rules checker program to access seventh and eighth threshold values stored in the memory device, wherein when the second input is low, the rules checker program determines the noise level on the second input and compares the determined noise level to the seventh threshold value, wherein when the second input is high, the rules checker program determines the noise level on the second input and compares the determined noise level to the eighth threshold value, the rules checker program using the results of the comparisons to determine whether or not the gate meets acceptable noise immunity requirements with respect to the fourth model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second, third and fourth models, the rules checker program determines that the gate has an acceptable noise immunity.

7. The apparatus of claim 1, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, wherein the rules checker program generates first, second, third and fourth models of the gate in order to process the widths of the P and N field effect transistors, the first, second, third and fourth models of the gate each consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a first ratio of the width of the P field

effect transistor of the first model to the width of the N field effect transistor of the first model, the rules checker program obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the rules checker program obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the rules checker program obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, wherein the rules checker program utilizes the largest and the smallest of all of the ratios to obtain first, second, third and fourth threshold values, respectively, from a memory device, the first and second threshold values corresponding to the largest of the ratios, the third and fourth threshold values corresponding to the smallest of the ratios, the threshold values being compared to noise levels on the inputs to determine whether or not the gate meets acceptable noise immunity requirements.

8. A method for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the method comprising the steps of:

receiving input in a computer relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors; and

analyzing the widths of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity.

9. The method of claim 8, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the analyzing step being performed by the rules checker program further comprising the steps of:

processing the widths of the P field effect transistor and of the N field effect transistor to obtain at least a first numerical value relating to the widths;

utilizing the first numerical value to access first and second threshold values stored in a memory device in communication with the computer;

determining noise levels on the input terminals; and

comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

10. The method of claim 9, wherein the processing step includes the step of generating a first model of the gate in order to process the widths of the P and N field effect transistors, the first model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the rules checker program to access the first and second threshold values stored in the memory device, wherein the rules checker program determines noise levels on the first and second inputs when the first and second inputs are high and compares the determined noise levels to the first and second threshold values, respectively, to determine whether or not the gate meets acceptable noise

immunity requirements with respect to the first model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first model, the rules checker program determines that the gate has an acceptable immunity to noise.

11. The method of claim 10, wherein the processing step further includes the step of generating a second model of the gate, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the rules checker program to access third and fourth threshold values stored in the memory device, wherein the rules checker program determines noise levels on the first and second inputs when the first and second inputs are low and compares the determined noise levels to the third and fourth threshold values, respectively, to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the rules checker program determines that the gate has an acceptable noise immunity.

12. The method of claim 11, wherein the wherein the processing step further includes the step of generating a third model of the gate, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a third ratio of the width of the P field effect transistor of the third model to the

width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the rules checker program to access fifth and sixth threshold values stored in the memory device, wherein the rules checker program determines the noise level on the first input when the first input is high and compares the determined noise level to the fifth and sixth threshold values, and wherein the rules checker program determines the noise level on the second input when the second input is high and compares the determined noise level to the fifth and sixth threshold values, the results of the comparison operations being used by the rules checker program to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the rules checker program determines that the gate has an acceptable noise immunity.

13. The method of claim 12, wherein the wherein the processing step further includes the step of generating a fourth model of the gate, the fourth model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, the fourth ratio corresponding to a fourth numerical value, the fourth numerical value being used by the rules checker program to access seventh and eighth threshold values stored in the memory device, wherein the rules checker program determines the noise level on the second input when the second input is low and compares the determined noise levels to the seventh and eighth threshold values, and wherein the rules checker program determines the noise level on the first input when the first input is low and compares the determined noise levels to the seventh and eighth threshold

values, the rules checker program using the results of the comparison operations to determine whether or not the gate meets acceptable noise immunity requirements with respect to the fourth model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second, third and fourth models, the rules checker program determines that the gate has an acceptable noise immunity.

14. The method of claim 9, wherein the processing step includes the step of generating first, second, third and fourth models of the gate in order to process the widths of the P and N field effect transistors, the first, second, third and fourth models of the gate each consisting of a single N field effect transistor and a single P field effect transistor, wherein during the processing step the rules checker program obtains first, second, third and fourth ratios, the first ratio corresponding to a ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value, the second ratio corresponding to a ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the third ratio corresponding to a ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the fourth ratio corresponding to a ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, wherein during the utilizing step the rules checker program utilizes the largest and the smallest of all of the ratios to obtain the first, second, third and fourth threshold values from the memory device, the first and second threshold values corresponding to the largest of the ratios, the third and fourth threshold values corresponding to the smallest of the ratios, the threshold values being compared to noise levels on the inputs of the gate for particular logic states, the results of the comparison

operations being utilized by the rules checker program to determine whether or not the gate meets acceptable noise immunity requirements.

15. A computer-readable medium containing a rules checker computer program, the computer program evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:

code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

16. (Once Amended) The computer-readable medium of claim 15, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the code comprising:

a first code segment which processes the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths;

a second code segment which utilizes the first numerical value to access first and second threshold values stored in a memory device in communication with the computer;

a third code segment which determines noise levels on the input terminals; and

a fourth code segment which compares the determined noise levels with the threshold values read out of the memory device and uses the results of the comparison tc determine whether or not the gate has an acceptable immunity to noise.

17. The computer-readable medium of claim 16, wherein the first code segment includes model generating code which generates a first model of the gate in order to process the widths of the P and N field effect transistors, the first model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the second code segment to access the first and second threshold values stored in the memory device, wherein when the first and second inputs are high, the third code segment determines noise levels on the first and second inputs and wherein the fourth code segment compares the determined noise levels to the first and second threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the first model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first model, the program determines that the gate has an acceptable immunity to noise.

18. The computer-readable medium of claim 17, wherein the model generating code generates a second model of the gate, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the second code segment to access a third and fourth threshold values stored in the memory device, wherein the third code segment determines noise levels on the first and second inputs when the first and second inputs are low and wherein the fourth code segment compares the determined noise levels to

the third and fourth threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the program determines that the gate has an acceptable noise immunity.

19. The computer-readable medium of claim 18, wherein the model generating code generates a third model of the gate, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the second code segment to access fifth and sixth threshold values stored in the memory device, wherein when the first input is high, the third code segment determines the noise level on the first input and wherein the fourth code segment compares the determined noise level to the fifth threshold value, and wherein when the first input is low, the third code segment determines the noise level on the first input and wherein the fourth code segment compares the determined noise level to the sixth threshold value, the fourth code segment using the results of the comparison operations to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the program determines that the gate has an acceptable noise immunity.

20. The computer-readable medium of claim 19, wherein the model generating code generates a fourth model of the gate, the fourth model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, the fourth ratio corresponding to a fourth numerical value, the fourth numerical value being used by the second code segment to access seventh and eighth threshold values stored in the memory device, wherein when the second input is low, the third code segment determines the noise level on the second input and wherein the fourth code segment compares the measured noise level to the seventh threshold value, and wherein when the second input is high, the third code segment determines the noise level on the second input and wherein the fourth code segment compares the measured noise level to the eighth threshold value, the fourth code segment using the results of the comparison to determine whether or not the gate meets acceptable noise immunity requirements with respect to the fourth model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first, second, third and fourth models, the program determines that the gate has an acceptable noise immunity.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claims 1-20 are pending in the application. The FINAL Office Action mailed April 24, 2002, rejected all claims 1-20. Specifically, claims 15-20 were rejected under 35 U.S.C. § 101. Claims 1-20 were rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent 5,446,674 to Ikeda et al. For the reasons set further herein, Applicants respectfully request that these rejections be overturned.

IV. STATUS OF AMENDMENTS

No amendments have been submitted after the FINAL Office Action, and all amendments submit prior to that have been entered.

V. SUMMARY OF THE INVENTION

The present invention provides a method and apparatus for evaluating a gate of an integrated circuit to determine whether or not the gate has acceptable immunity to noise. The apparatus comprises a computer configured to execute a rules checker program 100 which receives input relating to characteristics of a static gate 138 (or 163) contained in the integrated circuit. The gate 138 comprises at least two field effect transistors (FETs). Each FET has a width and the characteristics received in the input to the rules checker program 100 include the widths of the field effect transistors. The rules checker program 100 analyzes the widths of the FETs to determine whether or not the gate has an acceptable noise immunity.

Each gate typically comprises a plurality of FETs 139, 141, 142, 143, usually an NFET 142, 143 and a PFET 139, 141, and input terminals A, B for receiving input signals. The rules checker program 100 processes the widths of the PFETs 139, 141 and NFETs 142, 143 to obtain at least a first numerical value relating to the widths. The rules checker program 100 utilizes the first numerical value to access one or more threshold noise level values from a memory device in communication with the computer. The rules checker program determines noise levels on the inputs A, B, either through calculation or simulation. The rules checker program 100 compares the determined noise levels with the threshold values and uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

VI. CONCISE STATEMENT OF THE ISSUES PRESENTED FOR REVIEW

The issues in this appeal are: (1) whether claims 15-20 are unpatentable under 35 U.S.C. §101; and (2) whether claims 1-20 are unpatentable under 35 U.S.C. 102(b) over U.S. Patent 5,446,674 to Ikeda et al.

VII. GROUPING OF THE CLAIMS

The claims can generally be divided into ten (10) claim groupings, as set out below. For purposes of the argument set forth in this appeal brief, one claim from each group will be evaluated and discussed in connection with the prior art. The claim groups include:

(1) Claim Group I, which comprises claims 1, 7, 8, and 14;

(2) Claim Group II, which comprises claims 2 and 9;

(3) Claim Group III, which comprises claims 3 and 10;

(4) Claim Group IV, which comprises claims 4 and 11;

(5) Claim Group V, which comprises claims 5, 6, 12, and 13;

(6) Claim Group VI, which comprises claim 15;

(7) Claim Group VII, which comprises claim 16;

(8) Claim Group VIII, which comprises claim 17;

(9) Claim Group IX, which comprises claim 18; and

(10) Claim Group X, which comprises claims 19 and 20.

Reasons that Claim Groups Do Not Stand or Fall Together

Although, in reality, all claims of an application are distinct, Applicants have grouped the claims of the present application into ten distinct claim groups. One claim for each group has been chosen as the exemplary claim. The reason that the claims for any given group do not stand or fall with any claims of another group is, ultimately, because they are of differing scope. This differing scope is more specifically set out below.

In regard to Claim Group I, each of the claims 1, 7, 8, and 14 are directed to an apparatus for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise. The apparatus of claim 1 includes a rules checker program that analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity. Independent claim 1 is the representative claim of Claim Group I.

In regard to Claim Group II, each of the claims 2 and 9 further defines features of the gate of claim 1 (and 8). Should the Board determine that the narrowed features of the gate, as defined in claim 2 define this claim over the cited art reference, then claim 2 will stand or fall independently of the conclusion regarding claim 1.

In regard to Claim Group III, each of the claims 3 and 10 further defines features of the rules checker program of claim 2 (and 9). Should the Board determine that the narrowed

features of the rules checker program, as defined in claim 3 define this claim over the cited art reference, then claim 3 will stand or fall independently of the conclusion regarding the claims of Claim Groups I or II.

In regard to Claim Group IV, each of the claims 4 and 11 further defines features of the rules checker program of claim 3 (and 10). Should the Board determine that the narrowed features of the rules checker program, as defined in claim 4 define this claim over the cited art reference, then claim 4 will stand or fall independently of the conclusion regarding the claims of Claim Groups I, II or III.

In regard to Claim Group V, each of the claims 5, 6, 12, and 13 further defines features of the rules checker program of claim 4 (and 11). Should the Board determine that the narrowed features of the rules checker program, as defined in claim 5 define this claim over the cited art reference, then claim 5 will stand or fall independently of the conclusion regarding the claims of Claim Groups I, II, III, or IV.

In regard to Claim Groups VI through X, the claims in these claim groups loosely correspond to the claims of Claim Groups I through V, respectively. However, in addition to the substantive bases advanced by the Office Action for rejecting the claims of Claim Groups I through V, the Office Action also rejected the claims of Claim Groups VI through X under 35 U.S.C. § 101. Therefore, the claims of these claim groups could not be properly combined with the claims of Claim Groups I through V.

VIII. ARGUMENT

A. Fundamental Distinction of the Ikeda Patent

Applicant respectfully submits that the substantive rejections of claim 1-20 of the present application based upon Ikeda should be overturned, for reasons that will be

specifically discussed below. However, before addressing the details of the specific rejections, Applicant notes that there are fundamental differences between the system of Ikeda and the present invention. As summarized above, the present invention is directed to a method for evaluating a gate node to determine whether the gate node has been designed to have an acceptable level of noise immunity. The Ikeda patent only mentions the term "noise" in the context of crosstalk noise, and not in the manner taught and treated by the present invention.

In this regard, Ikeda recognizes that a transistor having low output impedance is prone to exert the influence of crosstalk on other wires. However, Ideka also recognizes that a transistor of high output impedance is susceptible to crosstalk from other wires. Accordingly, the system of the Ikeda patent is concerned with crosstalk verification. Furthermore, the system disclosed by Ikeda appears to reference wire patterns and the capacitance measurements therebetween to determine whether crosstalk noise will be problematic. These fundamental differences are embodied in the pending claims of the present application.

B. <u>Discussion of Claim Group I</u>

With regard to the claims of Claim Group I, the Office Action rejected claims 1, 7, 8, and 14 under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent 5,446,674 to Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

In rejecting claim 1, the Office Action stated:

> As per claims 1 and 15, Ikeda anticipated method and operation system for checking design rule as claimed. According to Ikeda, the method and system for design rule checker includes a computer configured to execute a rule checker program, wherein the design rule being checked for an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters

> such as width, length, connected in device channel, etc. ("Summary of the Invention", col. 1, line 44 to col. 2, line 24, col. 2, lines 24-53, col. 5, lines 18-56, col. 9, line 45 to col. 10, line 10). The program is designed to check transistor susceptible to noise in the cross-talk influence (col. 2, lines 7-24, col. 5, lines 18-56, col. 9, line 54-col 10, line 2), including checking noise susceptible or noise immunity as claimed for transistors to other transistors because they are parts of noise control scheme.

The undersigned has closely reviewed the Ikeda reference and submits that it does not disclose the invention as defined by the independent claim 1 of the present application.

Specifically, independent claim 1 recites:

> 1. An apparatus ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the apparatus comprising:
> a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, ***the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully submits that the rejection of claim 1 should be overturned for at least the reason that Ikeda fails to disclose or teach at least the features emphasized above.

As set forth above, Ikeda is directed to a crosstalk verification device. It operates by calculating the magnitude of ***crosstalk noise*** as a function of the wire-to-wire capacitance, in order to specify a portion in which the magnitude of crosstalk noise exceeds reference voltages (see e.g., col. 3, lines 46-60 and the Abstract of Ikeda).

In contrast, claim 1 specifies the analysis of widths of field effect transistors within a static gate, to determine whether the gate has an acceptable ***noise immunity***. Simply stated, Ikeda does not teach this claimed aspect, and therefore cannot form a proper anticipatory reference. Furthermore, the undersigned performed an electronic search of the entire text of

the Ikeda patent for the term "noise immunity" and this term is not mentioned anywhere within the Ikeda patent.

The Office Action cited col. 9, line 45 through col. 10, line 10 of Ikeda as allegedly teaching the claimed portion of the rules checker program that analyzes the widths of FETs to determine whether or not the gate has an acceptable level of noise immunity. In fact, this portion of Ikeda teaches the comparison of a width to length ratio (W/L) with a stored reference value to identify "the transistor prone to exert crosstalk influence and the transistor susceptible to crosstalk." (col. 9, line 68 through col. 10, line 1). In this respect, Ikeda teaches that a transistor with a low output impedance (W/L greater than first reference value) is prone to exert the influence of crosstalk, while a transistor of high output impedance (W/L less than second reference value) is susceptible to crosstalk. Again, and significantly, the assessment of the likelihood of exerting crosstalk or the susceptibility to crosstalk of the Ikeda patent is different than the assessment of noise immunity, as defined by claim 1 of the present application.

For at least the foregoing reasons, Applicant respectfully submits that the rejection of claim 1 (and 7, 8, and 14) is misplaced and should be overturned by the Board.

C. Discussion of Claim Group II

With regard to the claims of Claim Group II, the Office Action rejected claims 2 and 9 under 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

The Office Action rejected claim 2 stating only that:

> Ikeda anticipated reading transistor design parameters for design rule check as claimed. Such transistor circuit design would include for example inverter gate, p-channel and n-channel transistor, CMOS channel parameters, design parameters, etc. as well-known in transistor circuit design.

On its face, this rejection is legally deficient, because it fails to even allege all of the features that are defined in claim 2. In this regard, claim 2 recites:

> 2. The apparatus of claim 1, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, ***the rules checker program processing the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths, the rules checker program utilizing the first numerical value to access first and second threshold values stored in a memory device in communication with the computer***, the rules checker program determining noise levels on the inputs, the rules checker program comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

(*Emphasis added.*)

To constitute a proper anticipatory reference to claim 2, Ikeda must disclose every feature of claim 2. Ikeda fails to do this. More significantly, the Office Action has not even alleged that the features of claim 2 that have been emphasized above are disclosed in Ikeda. For this reason alone, the Examiner has failed to make a legally-proper, prima facie rejection of claim 2, and the Board should overturn the rejection. Furthermore, Applicant has reviewed the entirety of the Ikeda patent, and has failed to locate or identify any proper or legitimate disclosure of the elements emphasized above.

Accordingly, Applicant respectfully requests that the Board overturn the rejection of claim 2 (and 9).

D. Discussion of Claim Group III

With regard to the claims of Claim Group III, the Office Action rejected claims 3 and 10 under 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

The Office Action rejected claim 3 stating only that:

> As per claims 3-7, the rule checker program as in the art of record obtains transistor design parameters or extracting the design parameters as claimed, and checks with the operating conditions as claimed ("Summary of the Invention").

On its face, this rejection is legally deficient, because it fails to even allege all of the features that are defined in claim 3. In this regard, claim 3 recites:

> 3. The apparatus of claim 2, wherein ***the rules checker program generates a first model of the gate in order to process the widths of the P and N field effect transistors***, the first representation of the gate consisting of a single N field effect transistor and a single P field effect transistor, ***the rules checker program obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the rules checker program to access the first and second threshold values stored in the memory device***, wherein when the first and second inputs are high, ***the rules checker program determines noise levels on the first and second inputs and compares the determined noise levels to the first and second threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the first model***, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first model, the rules checker program determines that the gate has an acceptable immunity to noise.

(*Emphasis added.*)

To constitute a proper anticipatory reference to claim 3, Ikeda must disclose every feature of claim 3. Ikeda fails to do this. More significantly, the Office Action has not even alleged that the features of claim 3 that have been emphasized above are disclosed in Ikeda. For this reason alone, the Examiner has failed to make a legally-proper, prima facie rejection of claim 3, and the Board should overturn the rejection. Furthermore, Applicant has reviewed the entirety of the Ikeda patent, and has failed to locate or identify any proper or legitimate disclosure of the elements emphasized above.

Accordingly, Applicant respectfully requests that the Board overturn the rejection of claim 3 (and 10).

E. Discussion of Claim Group IV

With regard to the claims of Claim Group IV, the Office Action rejected claims 4 and 11 under 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

The Office Action rejected claim 4 stating only that:

> As per claims 3-7, the rule checker program as in the art of record obtains transistor design parameters or extracting the design parameters as claimed, and checks with the operating conditions as claimed ("Summary of the Invention").

On its face, this rejection is legally deficient, because it fails to even allege all of the features that are defined in claim 4. In this regard, claim 4 recites:

> 4. The apparatus of claim 3, wherein ***the rules checker program processes the widths of the P and N field effect transistors by generating a second model of the gate***, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, ***the rules checker program obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the rules checker program to access a third and fourth threshold values stored in the memory device***, wherein the rules checker program determines noise levels on the first and second inputs when the first and second inputs are low ***and compares the determined noise levels to the third and fourth threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model***, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the rules checker program determines that the gate has an acceptable noise immunity.

(*Emphasis added.*)

To constitute a proper anticipatory reference to claim 4, Ikeda must disclose every feature of claim 4. Ikeda fails to do this. More significantly, the Office Action has not even alleged that the features of claim 4 that have been emphasized above are disclosed in Ikeda. For example, claim 4 calls for the generation of a second model and the access of third and

forth threshold values, which are used to make the noise immunity determination. Simply state, Ikeda fails to disclose any of these features, nor does the Examiner make any specific allegations in this regard.

For this reason alone, the Examiner has failed to make a legally-proper, prima facie rejection of claim 4, and the Board should overturn the rejection. Furthermore, Applicant has reviewed the entirety of the Ikeda patent, and has failed to locate or identify any proper or legitimate disclosure of the elements emphasized above. Accordingly, Applicant respectfully requests that the Board overturn the rejection of claim 4 (and 11).

F. Discussion of Claim Group V

With regard to the claims of Claim Group V, the Office Action rejected claims 5, 6, 12 and 13 under 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

The Office Action rejected claim 5 stating only that:

> As per claims 3-7, the rule checker program as in the art of record obtains transistor design parameters or extracting the design parameters as claimed, and checks with the operating conditions as claimed ("Summary of the Invention").

On its face, this rejection is legally deficient, because it fails to even allege all of the features that are defined in claim 5. In this regard, claim 5 recites:

> 5. The apparatus of claim 4, wherein ***the rules checker program processes the widths of the P and N field effect transistors by generating a third model of the gate***, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, ***the rules checker program obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the rules checker program to access a fifth and sixth threshold values stored in the memory device***, wherein when the

> first input is high, the rules checker program determines the noise level on the first input and compares the determined noise level to the fifth threshold value, wherein when the first input is low, the rules checker program determines the noise level on the first input ***and compares the determined noise level to the sixth threshold value, wherein the results of the comparisons are used by the rules checker program to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model***, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the rules checker program determines that the gate has an acceptable noise immunity.

(*Emphasis added.*)

To constitute a proper anticipatory reference to claim 4, Ikeda must disclose every feature of claim 5. Ikeda fails to do this. More significantly, the Office Action has not even alleged that the features of claim 5 that have been emphasized above are disclosed in Ikeda. For example, claim 5 calls for the generation of a third model and the access of fifth and sixth threshold values, which are used to make the noise immunity determination. Simply stated, Ikeda fails to disclose any of these features, nor does the Examiner make any specific allegations in this regard.

For this reason alone, the Examiner has failed to make a legally-proper, prima facie rejection of claim 5, and the Board should overturn the rejection. Furthermore, Applicant has reviewed the entirety of the Ikeda patent, and has failed to locate or identify any proper or legitimate disclosure of the elements emphasized above. Accordingly, Applicant respectfully requests that the Board overturn the rejection of claim 5 (and 6, 12, and 13).

G. Discussion of Claim Group VI

With regard to the claim of Claim Group VI, the Office Action rejected claim 15 under both 35 U.S.C. § 101 as being directed to non-statutory subject matter and 35 U.S.C. §

102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

The Office Action rejected claim 15 under 35 U.S.C. § 101 alleging that "the claimed computer program ... is directed to a data structure [and] is necessarily to be converted into executable code and executed by a computer to meet statutory requirement." This rejection is just wrong, and is inconsistent with the prevailing case law as well as numerous other decisions made by the Patent Office. In this regard, the Federal Circuit has made clear that computer-readable media are legitimate statutory subject matter. Furthermore, the Patent Office Action has issued numerous patents with claims directed to "computer-readable mediums" set forth using the same language as Applicant has used for claim 15. The following is a list of just a few such patents (each issued on May 28, 2002):

U.S. Patent 6,397,381 (claim 1);
U.S. Patent 6,397,354 (claim 24);
U.S. Patent 6,397,352 (claim 14);
U.S. Patent 6,397,335 (claim 9);
U.S. Patent 6,397,208 (claim 7); and
U.S. Patent 6,397,169 (claim 7).

Therefore, as an administrative agency, which must act consistently from matter to matter and from applicant to applicant, the Patent Office must withdraw this rejection.

Furthermore, and more importantly, the rejection is misplaced and should be withdrawn. In this regard, Applicant respectfully submits that claim 15 is NOT directed to a data structure, but rather to a "computer-readable medium." In this regard, claim 15 recites:

> *15.* A ***computer-readable medium containing a rules checker computer program,*** the computer program evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:
>
> code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

As is clearly recited, the subject matter of claim 15 is directed to a computer-readable medium that "contains" a rules checker computer program. Therefore, claim 15 is properly directed to statutory subject matter (computer-readable media), and the rejection of claim 15 (as being directed to a data structure) is misplaced and should be overturned.

With regard to the substantive rejection of claim 15 (i.e., the rejection under 35 U.S.C. § 102(b) as anticipated by Ikeda), Applicant submits that the rejection of claim 15 should be overturned for the same reasons advanced above in connection with claim 1.

H. Discussion of Claim Group VII

With regard to the claim of Claim Group VII, the Office Action rejected claim 16 under both 35 U.S.C. § 101 as being directed to non-statutory subject matter and 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

With regard to the rejection under 35 U.S.C. § 101, Applicant respectfully submits that this rejection should be overturned for the same reason discussed above in connection with claim 15. With regard to the substantive rejection of claim 16 (i.e., the rejection under 35 U.S.C. § 102(b) as anticipated by Ikeda), Applicant submits that the rejection of claim 16 should be overturned for the same reasons advanced above in connection with claim 2.

Applicant has separated claim 16 into a separate claim group because it does not necessarily stand or fall with claim 2, due to the rejection under 35 U.S.C. § 101.

I. Discussion of Claim Group VIII

With regard to the claim of Claim Group VIII, the Office Action rejected claim 17 under both 35 U.S.C. § 101 as being directed to non-statutory subject matter and 35 U.S.C. §

102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

With regard to the rejection under 35 U.S.C. § 101, Applicant respectfully submits that this rejection should be overturned for the same reason discussed above in connection with claim 15. With regard to the substantive rejection of claim 17 (i.e., the rejection under 35 U.S.C. § 102(b) as anticipated by Ikeda), Applicant submits that the rejection of claim 17 should be overturned for the same reasons advanced above in connection with claim 3.

Applicant has separated claim 17 into a separate claim group because it does not necessarily stand or fall with claim 3, due to the rejection under 35 U.S.C. § 101.

J. Discussion of Claim Group IX

With regard to the claim of Claim Group IX, the Office Action rejected claim 18 under both 35 U.S.C. § 101 as being directed to non-statutory subject matter and 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

With regard to the rejection under 35 U.S.C. § 101, Applicant respectfully submits that this rejection should be overturned for the same reason discussed above in connection with claim 15. With regard to the substantive rejection of claim 18 (i.e., the rejection under 35 U.S.C. § 102(b) as anticipated by Ikeda), Applicant submits that the rejection of claim 18 should be overturned for the same reasons advanced above in connection with claim 4.

Applicant has separated claim 18 into a separate claim group because it does not necessarily stand or fall with claim 4, due to the rejection under 35 U.S.C. § 101.

K. Discussion of Claim Group X

With regard to the claims of Claim Group X, the Office Action rejected claims 19 and 20 under both 35 U.S.C. § 101 as being directed to non-statutory subject matter and 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

With regard to the rejection under 35 U.S.C. § 101, Applicant respectfully submits that this rejection should be overturned for the same reason discussed above in connection with claim 15. With regard to the substantive rejection of claim 19 (i.e., the rejection under 35 U.S.C. § 102(b) as anticipated by Ikeda), Applicant submits that the rejection of claim 10 should be overturned for the same reasons advanced above in connection with claim 5.

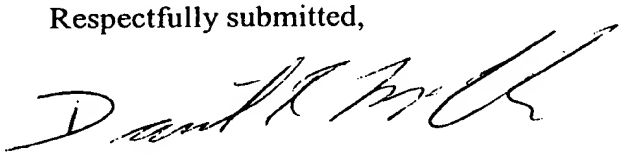
Applicant has separated claim 19 into a separate claim group because it does not necessarily stand or fall with claim 5, due to the rejection under 35 U.S.C. § 101.

IX. CONCLUSION

Based upon the foregoing discussion, Applicants respectfully requests that the Examiner's final rejection of claims 1-20 be overruled and withdrawn by the Board, and that the application be allowed to issue as a patent with all pending claims 1-20.

Please charge Hewlett-Packard Company's deposit account 08-2025 in the amount of $310 for the filing of this Appeal Brief. No additional fees are believed to be due in connection with this Appeal Brief. If, however, any additional fees are deemed to be payable, you are hereby authorized to charge any such fees to deposit account No. 08-2025.

Respectfully submitted,



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X. APPENDIX

Claims

1. An apparatus for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the apparatus comprising:

a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

2. The apparatus of claim 1, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the rules checker program processing the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths, the rules checker program utilizing the first numerical value to access first and second threshold values stored in a memory device in communication with the computer, the rules checker program determining noise levels on the inputs, the rules checker program comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

3. The apparatus of claim 2, wherein the rules checker program generates a first model of the gate in order to process the widths of the P and N field effect transistors, the first representation of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the rules checker program to access the first and second threshold values stored in the memory device, wherein when the first and second inputs are high, the rules checker program determines noise levels on the first and second inputs and compares the determined noise levels to the first and second threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the first model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first model, the rules checker program determines that the gate has an acceptable immunity to noise.

4. The apparatus of claim 3, wherein the rules checker program processes the widths of the P and N field effect transistors by generating a second model of the gate, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the rules checker program to access a third and fourth threshold values stored in the memory device, wherein the rules checker program determines noise levels on the first and second inputs when the first and second inputs are low and compares the

determined noise levels to the third and fourth threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the rules checker program determines that the gate has an acceptable noise immunity.

5. The apparatus of claim 4, wherein the rules checker program processes the widths of the P and N field effect transistors by generating a third model of the gate, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the rules checker program to access a fifth and sixth threshold values stored in the memory device, wherein when the first input is high, the rules checker program determines the noise level on the first input and compares the determined noise level to the fifth threshold value, wherein when the first input is low, the rules checker program determines the noise level on the first input and compares the determined noise level to the sixth threshold value, wherein the results of the comparisons are used by the rules checker program to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the rules checker program determines that the gate has an acceptable noise immunity.

6. The apparatus of claim 5, wherein the rules checker program processes the widths of the P and N field effect transistors by generating a fourth model of the gate, the fourth model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, the fourth ratio corresponding to a fourth numerical value, the fourth numerical value being used by the rules checker program to access seventh and eighth threshold values stored in the memory device, wherein when the second input is low, the rules checker program determines the noise level on the second input and compares the determined noise level to the seventh threshold value, wherein when the second input is high, the rules checker program determines the noise level on the second input and compares the determined noise level to the eighth threshold value, the rules checker program using the results of the comparisons to determine whether or not the gate meets acceptable noise immunity requirements with respect to the fourth model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second, third and fourth models, the rules checker program determines that the gate has an acceptable noise immunity.

7. The apparatus of claim 1, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, wherein the rules checker program generates first, second, third and fourth models of the gate in order to process the widths of the P and N field effect transistors, the first, second, third and fourth models of the gate each consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a first ratio of the width of the P field

effect transistor of the first model to the width of the N field effect transistor of the first model, the rules checker program obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the rules checker program obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the rules checker program obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, wherein the rules checker program utilizes the largest and the smallest of all of the ratios to obtain first, second, third and fourth threshold values, respectively, from a memory device, the first and second threshold values corresponding to the largest of the ratios, the third and fourth threshold values corresponding to the smallest of the ratios, the threshold values being compared to noise levels on the inputs to determine whether or not the gate meets acceptable noise immunity requirements.

8. A method for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the method comprising the steps of:

receiving input in a computer relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors; and

analyzing the widths of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity.

9. The method of claim 8, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the analyzing step being performed by the rules checker program further comprising the steps of:

processing the widths of the P field effect transistor and of the N field effect transistor to obtain at least a first numerical value relating to the widths;

utilizing the first numerical value to access first and second threshold values stored in a memory device in communication with the computer;

determining noise levels on the input terminals; and

comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

10. The method of claim 9, wherein the processing step includes the step of generating a first model of the gate in order to process the widths of the P and N field effect transistors, the first model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the rules checker program to access the first and second threshold values stored in the memory device, wherein the rules checker program determines noise levels on the first and second inputs when the first and second inputs are high and compares the determined noise levels to the first and second threshold values, respectively, to determine whether or not the gate meets acceptable noise

immunity requirements with respect to the first model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first model, the rules checker program determines that the gate has an acceptable immunity to noise.

11. The method of claim 10, wherein the processing step further includes the step of generating a second model of the gate, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the rules checker program to access third and fourth threshold values stored in the memory device, wherein the rules checker program determines noise levels on the first and second inputs when the first and second inputs are low and compares the determined noise levels to the third and fourth threshold values, respectively, to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the rules checker program determines that the gate has an acceptable noise immunity.

12. The method of claim 11, wherein the wherein the processing step further includes the step of generating a third model of the gate, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a third ratio of the width of the P field effect transistor of the third model to the

width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the rules checker program to access fifth and sixth threshold values stored in the memory device, wherein the rules checker program determines the noise level on the first input when the first input is high and compares the determined noise level to the fifth and sixth threshold values, and wherein the rules checker program determines the noise level on the second input when the second input is high and compares the determined noise level to the fifth and sixth threshold values, the results of the comparison operations being used by the rules checker program to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the rules checker program determines that the gate has an acceptable noise immunity.

13. The method of claim 12, wherein the wherein the processing step further includes the step of generating a fourth model of the gate, the fourth model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, the fourth ratio corresponding to a fourth numerical value, the fourth numerical value being used by the rules checker program to access seventh and eighth threshold values stored in the memory device, wherein the rules checker program determines the noise level on the second input when the second input is low and compares the determined noise levels to the seventh and eighth threshold values, and wherein the rules checker program determines the noise level on the first input when the first input is low and compares the determined noise levels to the seventh and eighth threshold

values, the rules checker program using the results of the comparison operations to determine whether or not the gate meets acceptable noise immunity requirements with respect to the fourth model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second, third and fourth models, the rules checker program determines that the gate has an acceptable noise immunity.

14. The method of claim 9, wherein the processing step includes the step of generating first, second, third and fourth models of the gate in order to process the widths of the P and N field effect transistors, the first, second, third and fourth models of the gate each consisting of a single N field effect transistor and a single P field effect transistor, wherein during the processing step the rules checker program obtains first, second, third and fourth ratios, the first ratio corresponding to a ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value, the second ratio corresponding to a ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the third ratio corresponding to a ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the fourth ratio corresponding to a ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, wherein during the utilizing step the rules checker program utilizes the largest and the smallest of all of the ratios to obtain the first, second, third and fourth threshold values from the memory device, the first and second threshold values corresponding to the largest of the ratios, the third and fourth threshold values corresponding to the smallest of the ratios, the threshold values being compared to noise levels on the inputs of the gate for particular logic states, the results of the comparison

operations being utilized by the rules checker program to determine whether or not the gate meets acceptable noise immunity requirements.

15. A computer-readable medium containing a rules checker computer program, the computer program evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:

code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

16. (Once Amended) The computer-readable medium of claim 15, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the code comprising:

a first code segment which processes the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths;

a second code segment which utilizes the first numerical value to access first and second threshold values stored in a memory device in communication with the computer;

a third code segment which determines noise levels on the input terminals; and

a fourth code segment which compares the determined noise levels with the threshold values read out of the memory device and uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

17. The computer-readable medium of claim 16, wherein the first code segment includes model generating code which generates a first model of the gate in order to process the widths of the P and N field effect transistors, the first model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the second code segment to access the first and second threshold values stored in the memory device, wherein when the first and second inputs are high, the third code segment determines noise levels on the first and second inputs and wherein the fourth code segment compares the determined noise levels to the first and second threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the first model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first model, the program determines that the gate has an acceptable immunity to noise.

18. The computer-readable medium of claim 17, wherein the model generating code generates a second model of the gate, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the second code segment to access a third and fourth threshold values stored in the memory device, wherein the third code segment determines noise levels on the first and second inputs when the first and second inputs are low and wherein the fourth code segment compares the determined noise levels to

the third and fourth threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the program determines that the gate has an acceptable noise immunity.

19. The computer-readable medium of claim 18, wherein the model generating code generates a third model of the gate, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the second code segment to access fifth and sixth threshold values stored in the memory device, wherein when the first input is high, the third code segment determines the noise level on the first input and wherein the fourth code segment compares the determined noise level to the fifth threshold value, and wherein when the first input is low, the third code segment determines the noise level on the first input and wherein the fourth code segment compares the determined noise level to the sixth threshold value, the fourth code segment using the results of the comparison operations to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the program determines that the gate has an acceptable noise immunity.

20. The computer-readable medium of claim 19, wherein the model generating code generates a fourth model of the gate, the fourth model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, the fourth ratio corresponding to a fourth numerical value, the fourth numerical value being used by the second code segment to access seventh and eighth threshold values stored in the memory device, wherein when the second input is low, the third code segment determines the noise level on the second input and wherein the fourth code segment compares the measured noise level to the seventh threshold value, and wherein when the second input is high, the third code segment determines the noise level on the second input and wherein the fourth code segment compares the measured noise level to the eighth threshold value, the fourth code segment using the results of the comparison to determine whether or not the gate meets acceptable noise immunity requirements with respect to the fourth model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first, second, third and fourth models, the program determines that the gate has an acceptable noise immunity.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:	)	
	)	
John G. McBride	)	Group Art Unit: 2123
	)	
Serial No.: 09/273,784	)	Examiner: Phan, T.
	)	
Filed: March 22, 1999	)	HP Docket No. 10971308-1
	)	TKHR Dkt. No. 50814-1470
	)	
For: METHOD AND APPARATUS FOR EVALUATING THE QUALITY OF NETWORK NODES	)	

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CERTIFICATE OF MAILING

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Signature – Hui Chin Barnhill

APPEAL BRIEF UNDER 37 C.F.R. §1.192

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

This is an appeal from the decision of Examiner Thai Phan, Group Art Unit 2123, of April 24, 2002 (Paper No. 7), rejecting claims 1-20 in the present application and making the rejection FINAL.

I. REAL PARTY IN INTEREST

The real party in interest of the instant application is Hewlett-Packard Company, a Delaware corporation, having its principal place of business in Palo Alto, California.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claims 1-20 are pending in the application. The FINAL Office Action mailed April 24, 2002, rejected all claims 1-20. Specifically, claims 15-20 were rejected under 35 U.S.C. § 101. Claims 1-20 were rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent 5,446,674 to Ikeda et al. For the reasons set further herein, Applicants respectfully request that these rejections be overturned.

IV. STATUS OF AMENDMENTS

No amendments have been submitted after the FINAL Office Action, and all amendments submit prior to that have been entered.

V. SUMMARY OF THE INVENTION

The present invention provides a method and apparatus for evaluating a gate of an integrated circuit to determine whether or not the gate has acceptable immunity to noise. The apparatus comprises a computer configured to execute a rules checker program 100 which receives input relating to characteristics of a static gate 138 (or 163) contained in the integrated circuit. The gate 138 comprises at least two field effect transistors (FETs). Each FET has a width and the characteristics received in the input to the rules checker program 100 include the widths of the field effect transistors. The rules checker program 100 analyzes the widths of the FETs to determine whether or not the gate has an acceptable noise immunity.

Each gate typically comprises a plurality of FETs 139, 141, 142, 143, usually an NFET 142, 143 and a PFET 139, 141, and input terminals A, B for receiving input signals. The rules checker program 100 processes the widths of the PFETs 139, 141 and NFETs 142, 143 to obtain at least a first numerical value relating to the widths. The rules checker program 100 utilizes the first numerical value to access one or more threshold noise level values from a memory device in communication with the computer. The rules checker program determines noise levels on the inputs A, B, either through calculation or simulation. The rules checker program 100 compares the determined noise levels with the threshold values and uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

VI. CONCISE STATEMENT OF THE ISSUES PRESENTED FOR REVIEW

The issues in this appeal are: (1) whether claims 15-20 are unpatentable under 35 U.S.C. §101; and (2) whether claims 1-20 are unpatentable under 35 U.S.C. 102(b) over U.S. Patent 5,446,674 to Ikeda et al.

VII. GROUPING OF THE CLAIMS

The claims can generally be divided into ten (10) claim groupings, as set out below. For purposes of the argument set forth in this appeal brief, one claim from each group will be evaluated and discussed in connection with the prior art. The claim groups include:

(1) Claim Group I, which comprises claims 1, 7, 8, and 14;

(2) Claim Group II, which comprises claims 2 and 9;

(3) Claim Group III, which comprises claims 3 and 10;

(4) Claim Group IV, which comprises claims 4 and 11;

(5) Claim Group V, which comprises claims 5, 6, 12, and 13;

(6) Claim Group VI, which comprises claim 15;

(7) Claim Group VII, which comprises claim 16;

(8) Claim Group VIII, which comprises claim 17;

(9) Claim Group IX, which comprises claim 18; and

(10) Claim Group X, which comprises claims 19 and 20.

Reasons that Claim Groups Do Not Stand or Fall Together

Although, in reality, all claims of an application are distinct, Applicants have grouped the claims of the present application into ten distinct claim groups. One claim for each group has been chosen as the exemplary claim. The reason that the claims for any given group do not stand or fall with any claims of another group is, ultimately, because they are of differing scope. This differing scope is more specifically set out below.

In regard to Claim Group I, each of the claims 1, 7, 8, and 14 are directed to an apparatus for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise. The apparatus of claim 1 includes a rules checker program that analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity. Independent claim 1 is the representative claim of Claim Group I.

In regard to Claim Group II, each of the claims 2 and 9 further defines features of the gate of claim 1 (and 8). Should the Board determine that the narrowed features of the gate, as defined in claim 2 define this claim over the cited art reference, then claim 2 will stand or fall independently of the conclusion regarding claim 1.

In regard to Claim Group III, each of the claims 3 and 10 further defines features of the rules checker program of claim 2 (and 9). Should the Board determine that the narrowed

features of the rules checker program, as defined in claim 3 define this claim over the cited art reference, then claim 3 will stand or fall independently of the conclusion regarding the claims of Claim Groups I or II.

In regard to Claim Group IV, each of the claims 4 and 11 further defines features of the rules checker program of claim 3 (and 10). Should the Board determine that the narrowed features of the rules checker program, as defined in claim 4 define this claim over the cited art reference, then claim 4 will stand or fall independently of the conclusion regarding the claims of Claim Groups I, II or III.

In regard to Claim Group V, each of the claims 5, 6, 12, and 13 further defines features of the rules checker program of claim 4 (and 11). Should the Board determine that the narrowed features of the rules checker program, as defined in claim 5 define this claim over the cited art reference, then claim 5 will stand or fall independently of the conclusion regarding the claims of Claim Groups I, II, III, or IV.

In regard to Claim Groups VI through X, the claims in these claim groups loosely correspond to the claims of Claim Groups I through V, respectively. However, in addition to the substantive bases advanced by the Office Action for rejecting the claims of Claim Groups I through V, the Office Action also rejected the claims of Claim Groups VI through X under 35 U.S.C. § 101. Therefore, the claims of these claim groups could not be properly combined with the claims of Claim Groups I through V.

VIII. ARGUMENT

A. Fundamental Distinction of the Ikeda Patent

Applicant respectfully submits that the substantive rejections of claim 1-20 of the present application based upon Ikeda should be overturned, for reasons that will be

specifically discussed below. However, before addressing the details of the specific rejections, Applicant notes that there are fundamental differences between the system of Ikeda and the present invention. As summarized above, the present invention is directed to a method for evaluating a gate node to determine whether the gate node has been designed to have an acceptable level of noise immunity. The Ikeda patent only mentions the term "noise" in the context of crosstalk noise, and not in the manner taught and treated by the present invention.

In this regard, Ikeda recognizes that a transistor having low output impedance is prone to exert the influence of crosstalk on other wires. However, Ideka also recognizes that a transistor of high output impedance is susceptible to crosstalk from other wires. Accordingly, the system of the Ikeda patent is concerned with crosstalk verification. Furthermore, the system disclosed by Ikeda appears to reference wire patterns and the capacitance measurements therebetween to determine whether crosstalk noise will be problematic. These fundamental differences are embodied in the pending claims of the present application.

B. Discussion of Claim Group I

With regard to the claims of Claim Group I, the Office Action rejected claims 1, 7, 8, and 14 under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent 5,446,674 to Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

In rejecting claim 1, the Office Action stated:

> As per claims 1 and 15, Ikeda anticipated method and operation system for checking design rule as claimed. According to Ikeda, the method and system for design rule checker includes a computer configured to execute a rule checker program, wherein the design rule being checked for an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters

> such as width, length, connected in device channel, etc. ("Summary of the Invention", col. 1, line 44 to col. 2, line 24, col. 2, lines 24-53, col. 5, lines 18-56, col. 9, line 45 to col. 10, line 10). The program is designed to check transistor susceptible to noise in the cross-talk influence (col. 2, lines 7-24, col. 5, lines 18-56, col. 9, line 54-col 10, line 2), including checking noise susceptible or noise immunity as claimed for transistors to other transistors because they are parts of noise control scheme.

The undersigned has closely reviewed the Ikeda reference and submits that it does not disclose the invention as defined by the independent claim 1 of the present application.

Specifically, independent claim 1 recites:

> 1. An apparatus ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the apparatus comprising:
> a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, ***the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully submits that the rejection of claim 1 should be overturned for at least the reason that Ikeda fails to disclose or teach at least the features emphasized above.

As set forth above, Ikeda is directed to a crosstalk verification device. It operates by calculating the magnitude of ***crosstalk noise*** as a function of the wire-to-wire capacitance, in order to specify a portion in which the magnitude of crosstalk noise exceeds reference voltages (see e.g., col. 3, lines 46-60 and the Abstract of Ikeda).

In contrast, claim 1 specifies the analysis of widths of field effect transistors within a static gate, to determine whether the gate has an acceptable ***noise immunity***. Simply stated, Ikeda does not teach this claimed aspect, and therefore cannot form a proper anticipatory reference. Furthermore, the undersigned performed an electronic search of the entire text of

the Ikeda patent for the term "noise immunity" and this term is not mentioned anywhere within the Ikeda patent.

The Office Action cited col. 9, line 45 through col. 10, line 10 of Ikeda as allegedly teaching the claimed portion of the rules checker program that analyzes the widths of FETs to determine whether or not the gate has an acceptable level of noise immunity. In fact, this portion of Ikeda teaches the comparison of a width to length ratio (W/L) with a stored reference value to identify "the transistor prone to exert crosstalk influence and the transistor susceptible to crosstalk." (col. 9, line 68 through col. 10, line 1). In this respect, Ikeda teaches that a transistor with a low output impedance (W/L greater than first reference value) is prone to exert the influence of crosstalk, while a transistor of high output impedance (W/L less than second reference value) is susceptible to crosstalk. Again, and significantly, the assessment of the likelihood of exerting crosstalk or the susceptibility to crosstalk of the Ikeda patent is different than the assessment of noise immunity, as defined by claim 1 of the present application.

For at least the foregoing reasons, Applicant respectfully submits that the rejection of claim 1 (and 7, 8, and 14) is misplaced and should be overturned by the Board.

C. Discussion of Claim Group II

With regard to the claims of Claim Group II, the Office Action rejected claims 2 and 9 under 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

The Office Action rejected claim 2 stating only that:

> Ikeda anticipated reading transistor design parameters for design rule check as claimed. Such transistor circuit design would include for example inverter gate, p-channel and n-channel transistor, CMOS channel parameters, design parameters, etc. as well-known in transistor circuit design.

On its face, this rejection is legally deficient, because it fails to even allege all of the features that are defined in claim 2. In this regard, claim 2 recites:

> 2. The apparatus of claim 1, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, ***the rules checker program processing the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths, the rules checker program utilizing the first numerical value to access first and second threshold values stored in a memory device in communication with the computer***, the rules checker program determining noise levels on the inputs, the rules checker program comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

(*Emphasis added.*)

To constitute a proper anticipatory reference to claim 2, Ikeda must disclose every feature of claim 2. Ikeda fails to do this. More significantly, the Office Action has not even alleged that the features of claim 2 that have been emphasized above are disclosed in Ikeda. For this reason alone, the Examiner has failed to make a legally-proper, prima facie rejection of claim 2, and the Board should overturn the rejection. Furthermore, Applicant has reviewed the entirety of the Ikeda patent, and has failed to locate or identify any proper or legitimate disclosure of the elements emphasized above.

Accordingly, Applicant respectfully requests that the Board overturn the rejection of claim 2 (and 9).

D. Discussion of Claim Group III

With regard to the claims of Claim Group III, the Office Action rejected claims 3 and 10 under 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

The Office Action rejected claim 3 stating only that:

> As per claims 3-7, the rule checker program as in the art of record obtains transistor design parameters or extracting the design parameters as claimed, and checks with the operating conditions as claimed ("Summary of the Invention").

On its face, this rejection is legally deficient, because it fails to even allege all of the features that are defined in claim 3. In this regard, claim 3 recites:

> 3. The apparatus of claim 2, wherein ***the rules checker program generates a first model of the gate in order to process the widths of the P and N field effect transistors***, the first representation of the gate consisting of a single N field effect transistor and a single P field effect transistor, ***the rules checker program obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the rules checker program to access the first and second threshold values stored in the memory device***, wherein when the first and second inputs are high, ***the rules checker program determines noise levels on the first and second inputs and compares the determined noise levels to the first and second threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the first model***, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first model, the rules checker program determines that the gate has an acceptable immunity to noise.

(*Emphasis added.*)

To constitute a proper anticipatory reference to claim 3, Ikeda must disclose every feature of claim 3. Ikeda fails to do this. More significantly, the Office Action has not even alleged that the features of claim 3 that have been emphasized above are disclosed in Ikeda. For this reason alone, the Examiner has failed to make a legally-proper, prima facie rejection of claim 3, and the Board should overturn the rejection. Furthermore, Applicant has reviewed the entirety of the Ikeda patent, and has failed to locate or identify any proper or legitimate disclosure of the elements emphasized above.

Accordingly, Applicant respectfully requests that the Board overturn the rejection of claim 3 (and 10).

E. Discussion of Claim Group IV

With regard to the claims of Claim Group IV, the Office Action rejected claims 4 and 11 under 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

The Office Action rejected claim 4 stating only that:

> As per claims 3-7, the rule checker program as in the art of record obtains transistor design parameters or extracting the design parameters as claimed, and checks with the operating conditions as claimed ("Summary of the Invention").

On its face, this rejection is legally deficient, because it fails to even allege all of the features that are defined in claim 4. In this regard, claim 4 recites:

> 4. The apparatus of claim 3, wherein ***the rules checker program processes the widths of the P and N field effect transistors by generating a second model of the gate***, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, ***the rules checker program obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the rules checker program to access a third and fourth threshold values stored in the memory device***, wherein the rules checker program determines noise levels on the first and second inputs when the first and second inputs are low ***and compares the determined noise levels to the third and fourth threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model***, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the rules checker program determines that the gate has an acceptable noise immunity.

(*Emphasis added.*)

To constitute a proper anticipatory reference to claim 4, Ikeda must disclose every feature of claim 4. Ikeda fails to do this. More significantly, the Office Action has not even alleged that the features of claim 4 that have been emphasized above are disclosed in Ikeda. For example, claim 4 calls for the generation of a second model and the access of third and

forth threshold values, which are used to make the noise immunity determination. Simply state, Ikeda fails to disclose any of these features, nor does the Examiner make any specific allegations in this regard.

For this reason alone, the Examiner has failed to make a legally-proper, prima facie rejection of claim 4, and the Board should overturn the rejection. Furthermore, Applicant has reviewed the entirety of the Ikeda patent, and has failed to locate or identify any proper or legitimate disclosure of the elements emphasized above. Accordingly, Applicant respectfully requests that the Board overturn the rejection of claim 4 (and 11).

F. Discussion of Claim Group V

With regard to the claims of Claim Group V, the Office Action rejected claims 5, 6, 12 and 13 under 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

The Office Action rejected claim 5 stating only that:

> As per claims 3-7, the rule checker program as in the art of record obtains transistor design parameters or extracting the design parameters as claimed, and checks with the operating conditions as claimed ("Summary of the Invention").

On its face, this rejection is legally deficient, because it fails to even allege all of the features that are defined in claim 5. In this regard, claim 5 recites:

> 5. The apparatus of claim 4, wherein ***the rules checker program processes the widths of the P and N field effect transistors by generating a third model of the gate***, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, ***the rules checker program obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the rules checker program to access a fifth and sixth threshold values stored in the memory device***, wherein when the

> first input is high, the rules checker program determines the noise level on the first input and compares the determined noise level to the fifth threshold value, wherein when the first input is low, the rules checker program determines the noise level on the first input ***and compares the determined noise level to the sixth threshold value, wherein the results of the comparisons are used by the rules checker program to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model***, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the rules checker program determines that the gate has an acceptable noise immunity.

(*Emphasis added.*)

To constitute a proper anticipatory reference to claim 4, Ikeda must disclose every feature of claim 5. Ikeda fails to do this. More significantly, the Office Action has not even alleged that the features of claim 5 that have been emphasized above are disclosed in Ikeda. For example, claim 5 calls for the generation of a third model and the access of fifth and sixth threshold values, which are used to make the noise immunity determination. Simply stated, Ikeda fails to disclose any of these features, nor does the Examiner make any specific allegations in this regard.

For this reason alone, the Examiner has failed to make a legally-proper, prima facie rejection of claim 5, and the Board should overturn the rejection. Furthermore, Applicant has reviewed the entirety of the Ikeda patent, and has failed to locate or identify any proper or legitimate disclosure of the elements emphasized above. Accordingly, Applicant respectfully requests that the Board overturn the rejection of claim 5 (and 6, 12, and 13).

G. Discussion of Claim Group VI

With regard to the claim of Claim Group VI, the Office Action rejected claim 15 under both 35 U.S.C. § 101 as being directed to non-statutory subject matter and 35 U.S.C. §

102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

The Office Action rejected claim 15 under 35 U.S.C. § 101 alleging that "the claimed computer program ... is directed to a data structure [and] is necessarily to be converted into executable code and executed by a computer to meet statutory requirement." This rejection is just wrong, and is inconsistent with the prevailing case law as well as numerous other decisions made by the Patent Office. In this regard, the Federal Circuit has made clear that computer-readable media are legitimate statutory subject matter. Furthermore, the Patent Office Action has issued numerous patents with claims directed to "computer-readable mediums" set forth using the same language as Applicant has used for claim 15. The following is a list of just a few such patents (each issued on May 28, 2002):

U.S. Patent 6,397,381 (claim 1);
U.S. Patent 6,397,354 (claim 24);
U.S. Patent 6,397,352 (claim 14);
U.S. Patent 6,397,335 (claim 9);
U.S. Patent 6,397,208 (claim 7); and
U.S. Patent 6,397,169 (claim 7).

Therefore, as an administrative agency, which must act consistently from matter to matter and from applicant to applicant, the Patent Office must withdraw this rejection.

Furthermore, and more importantly, the rejection is misplaced and should be withdrawn. In this regard, Applicant respectfully submits that claim 15 is NOT directed to a data structure, but rather to a "computer-readable medium." In this regard, claim 15 recites:

> *15.* A ***computer-readable medium containing a rules checker computer program,*** the computer program evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:
>
> code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

As is clearly recited, the subject matter of claim 15 is directed to a computer-readable medium that "contains" a rules checker computer program. Therefore, claim 15 is properly directed to statutory subject matter (computer-readable media), and the rejection of claim 15 (as being directed to a data structure) is misplaced and should be overturned.

With regard to the substantive rejection of claim 15 (i.e., the rejection under 35 U.S.C. § 102(b) as anticipated by Ikeda), Applicant submits that the rejection of claim 15 should be overturned for the same reasons advanced above in connection with claim 1.

H. Discussion of Claim Group VII

With regard to the claim of Claim Group VII, the Office Action rejected claim 16 under both 35 U.S.C. § 101 as being directed to non-statutory subject matter and 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

With regard to the rejection under 35 U.S.C. § 101, Applicant respectfully submits that this rejection should be overturned for the same reason discussed above in connection with claim 15. With regard to the substantive rejection of claim 16 (i.e., the rejection under 35 U.S.C. § 102(b) as anticipated by Ikeda), Applicant submits that the rejection of claim 16 should be overturned for the same reasons advanced above in connection with claim 2.

Applicant has separated claim 16 into a separate claim group because it does not necessarily stand or fall with claim 2, due to the rejection under 35 U.S.C. § 101.

I. Discussion of Claim Group VIII

With regard to the claim of Claim Group VIII, the Office Action rejected claim 17 under both 35 U.S.C. § 101 as being directed to non-statutory subject matter and 35 U.S.C. §

102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

With regard to the rejection under 35 U.S.C. § 101, Applicant respectfully submits that this rejection should be overturned for the same reason discussed above in connection with claim 15. With regard to the substantive rejection of claim 17 (i.e., the rejection under 35 U.S.C. § 102(b) as anticipated by Ikeda), Applicant submits that the rejection of claim 17 should be overturned for the same reasons advanced above in connection with claim 3.

Applicant has separated claim 17 into a separate claim group because it does not necessarily stand or fall with claim 3, due to the rejection under 35 U.S.C. § 101.

J. Discussion of Claim Group IX

With regard to the claim of Claim Group IX, the Office Action rejected claim 18 under both 35 U.S.C. § 101 as being directed to non-statutory subject matter and 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

With regard to the rejection under 35 U.S.C. § 101, Applicant respectfully submits that this rejection should be overturned for the same reason discussed above in connection with claim 15. With regard to the substantive rejection of claim 18 (i.e., the rejection under 35 U.S.C. § 102(b) as anticipated by Ikeda), Applicant submits that the rejection of claim 18 should be overturned for the same reasons advanced above in connection with claim 4.

Applicant has separated claim 18 into a separate claim group because it does not necessarily stand or fall with claim 4, due to the rejection under 35 U.S.C. § 101.

K. Discussion of Claim Group X

With regard to the claims of Claim Group X, the Office Action rejected claims 19 and 20 under both 35 U.S.C. § 101 as being directed to non-statutory subject matter and 35 U.S.C. § 102(b), as being anticipated by Ikeda et al. Applicant respectfully submits that this rejection should be overturned for at least the reasons that follow.

With regard to the rejection under 35 U.S.C. § 101, Applicant respectfully submits that this rejection should be overturned for the same reason discussed above in connection with claim 15. With regard to the substantive rejection of claim 19 (i.e., the rejection under 35 U.S.C. § 102(b) as anticipated by Ikeda), Applicant submits that the rejection of claim 10 should be overturned for the same reasons advanced above in connection with claim 5.

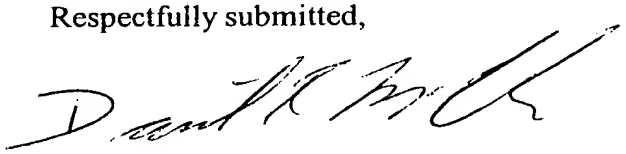
Applicant has separated claim 19 into a separate claim group because it does not necessarily stand or fall with claim 5, due to the rejection under 35 U.S.C. § 101.

IX. CONCLUSION

Based upon the foregoing discussion, Applicants respectfully requests that the Examiner's final rejection of claims 1-20 be overruled and withdrawn by the Board, and that the application be allowed to issue as a patent with all pending claims 1-20.

Please charge Hewlett-Packard Company's deposit account 08-2025 in the amount of $310 for the filing of this Appeal Brief. No additional fees are believed to be due in connection with this Appeal Brief. If, however, any additional fees are deemed to be payable, you are hereby authorized to charge any such fees to deposit account No. 08-2025.

Respectfully submitted,



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X. APPENDIX

Claims

1. An apparatus for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the apparatus comprising:

a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

2. The apparatus of claim 1, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the rules checker program processing the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths, the rules checker program utilizing the first numerical value to access first and second threshold values stored in a memory device in communication with the computer, the rules checker program determining noise levels on the inputs, the rules checker program comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

3. The apparatus of claim 2, wherein the rules checker program generates a first model of the gate in order to process the widths of the P and N field effect transistors, the first representation of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the rules checker program to access the first and second threshold values stored in the memory device, wherein when the first and second inputs are high, the rules checker program determines noise levels on the first and second inputs and compares the determined noise levels to the first and second threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the first model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first model, the rules checker program determines that the gate has an acceptable immunity to noise.

4. The apparatus of claim 3, wherein the rules checker program processes the widths of the P and N field effect transistors by generating a second model of the gate, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the rules checker program to access a third and fourth threshold values stored in the memory device, wherein the rules checker program determines noise levels on the first and second inputs when the first and second inputs are low and compares the

determined noise levels to the third and fourth threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the rules checker program determines that the gate has an acceptable noise immunity.

5. The apparatus of claim 4, wherein the rules checker program processes the widths of the P and N field effect transistors by generating a third model of the gate, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the rules checker program to access a fifth and sixth threshold values stored in the memory device, wherein when the first input is high, the rules checker program determines the noise level on the first input and compares the determined noise level to the fifth threshold value, wherein when the first input is low, the rules checker program determines the noise level on the first input and compares the determined noise level to the sixth threshold value, wherein the results of the comparisons are used by the rules checker program to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the rules checker program determines that the gate has an acceptable noise immunity.

6. The apparatus of claim 5, wherein the rules checker program processes the widths of the P and N field effect transistors by generating a fourth model of the gate, the fourth model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, the fourth ratio corresponding to a fourth numerical value, the fourth numerical value being used by the rules checker program to access seventh and eighth threshold values stored in the memory device, wherein when the second input is low, the rules checker program determines the noise level on the second input and compares the determined noise level to the seventh threshold value, wherein when the second input is high, the rules checker program determines the noise level on the second input and compares the determined noise level to the eighth threshold value, the rules checker program using the results of the comparisons to determine whether or not the gate meets acceptable noise immunity requirements with respect to the fourth model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second, third and fourth models, the rules checker program determines that the gate has an acceptable noise immunity.

7. The apparatus of claim 1, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, wherein the rules checker program generates first, second, third and fourth models of the gate in order to process the widths of the P and N field effect transistors, the first, second, third and fourth models of the gate each consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a first ratio of the width of the P field

effect transistor of the first model to the width of the N field effect transistor of the first model, the rules checker program obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the rules checker program obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the rules checker program obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, wherein the rules checker program utilizes the largest and the smallest of all of the ratios to obtain first, second, third and fourth threshold values, respectively, from a memory device, the first and second threshold values corresponding to the largest of the ratios, the third and fourth threshold values corresponding to the smallest of the ratios, the threshold values being compared to noise levels on the inputs to determine whether or not the gate meets acceptable noise immunity requirements.

8. A method for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the method comprising the steps of:

receiving input in a computer relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors; and

analyzing the widths of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity.

9. The method of claim 8, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the analyzing step being performed by the rules checker program further comprising the steps of:

processing the widths of the P field effect transistor and of the N field effect transistor to obtain at least a first numerical value relating to the widths;

utilizing the first numerical value to access first and second threshold values stored in a memory device in communication with the computer;

determining noise levels on the input terminals; and

comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

10. The method of claim 9, wherein the processing step includes the step of generating a first model of the gate in order to process the widths of the P and N field effect transistors, the first model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the rules checker program to access the first and second threshold values stored in the memory device, wherein the rules checker program determines noise levels on the first and second inputs when the first and second inputs are high and compares the determined noise levels to the first and second threshold values, respectively, to determine whether or not the gate meets acceptable noise

immunity requirements with respect to the first model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first model, the rules checker program determines that the gate has an acceptable immunity to noise.

11. The method of claim 10, wherein the processing step further includes the step of generating a second model of the gate, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the rules checker program to access third and fourth threshold values stored in the memory device, wherein the rules checker program determines noise levels on the first and second inputs when the first and second inputs are low and compares the determined noise levels to the third and fourth threshold values, respectively, to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the rules checker program determines that the gate has an acceptable noise immunity.

12. The method of claim 11, wherein the wherein the processing step further includes the step of generating a third model of the gate, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a third ratio of the width of the P field effect transistor of the third model to the

width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the rules checker program to access fifth and sixth threshold values stored in the memory device, wherein the rules checker program determines the noise level on the first input when the first input is high and compares the determined noise level to the fifth and sixth threshold values, and wherein the rules checker program determines the noise level on the second input when the second input is high and compares the determined noise level to the fifth and sixth threshold values, the results of the comparison operations being used by the rules checker program to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the rules checker program determines that the gate has an acceptable noise immunity.

13. The method of claim 12, wherein the wherein the processing step further includes the step of generating a fourth model of the gate, the fourth model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, the fourth ratio corresponding to a fourth numerical value, the fourth numerical value being used by the rules checker program to access seventh and eighth threshold values stored in the memory device, wherein the rules checker program determines the noise level on the second input when the second input is low and compares the determined noise levels to the seventh and eighth threshold values, and wherein the rules checker program determines the noise level on the first input when the first input is low and compares the determined noise levels to the seventh and eighth threshold

values, the rules checker program using the results of the comparison operations to determine whether or not the gate meets acceptable noise immunity requirements with respect to the fourth model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second, third and fourth models, the rules checker program determines that the gate has an acceptable noise immunity.

14. The method of claim 9, wherein the processing step includes the step of generating first, second, third and fourth models of the gate in order to process the widths of the P and N field effect transistors, the first, second, third and fourth models of the gate each consisting of a single N field effect transistor and a single P field effect transistor, wherein during the processing step the rules checker program obtains first, second, third and fourth ratios, the first ratio corresponding to a ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value, the second ratio corresponding to a ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the third ratio corresponding to a ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the fourth ratio corresponding to a ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, wherein during the utilizing step the rules checker program utilizes the largest and the smallest of all of the ratios to obtain the first, second, third and fourth threshold values from the memory device, the first and second threshold values corresponding to the largest of the ratios, the third and fourth threshold values corresponding to the smallest of the ratios, the threshold values being compared to noise levels on the inputs of the gate for particular logic states, the results of the comparison

operations being utilized by the rules checker program to determine whether or not the gate meets acceptable noise immunity requirements.

15. A computer-readable medium containing a rules checker computer program, the computer program evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:

code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

16. (Once Amended) The computer-readable medium of claim 15, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the code comprising:

a first code segment which processes the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths;

a second code segment which utilizes the first numerical value to access first and second threshold values stored in a memory device in communication with the computer;

a third code segment which determines noise levels on the input terminals; and

a fourth code segment which compares the determined noise levels with the threshold values read out of the memory device and uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

17. The computer-readable medium of claim 16, wherein the first code segment includes model generating code which generates a first model of the gate in order to process the widths of the P and N field effect transistors, the first model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the second code segment to access the first and second threshold values stored in the memory device, wherein when the first and second inputs are high, the third code segment determines noise levels on the first and second inputs and wherein the fourth code segment compares the determined noise levels to the first and second threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the first model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first model, the program determines that the gate has an acceptable immunity to noise.

18. The computer-readable medium of claim 17, wherein the model generating code generates a second model of the gate, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the second code segment to access a third and fourth threshold values stored in the memory device, wherein the third code segment determines noise levels on the first and second inputs when the first and second inputs are low and wherein the fourth code segment compares the determined noise levels to

the third and fourth threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the program determines that the gate has an acceptable noise immunity.

19. The computer-readable medium of claim 18, wherein the model generating code generates a third model of the gate, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the second code segment to access fifth and sixth threshold values stored in the memory device, wherein when the first input is high, the third code segment determines the noise level on the first input and wherein the fourth code segment compares the determined noise level to the fifth threshold value, and wherein when the first input is low, the third code segment determines the noise level on the first input and wherein the fourth code segment compares the determined noise level to the sixth threshold value, the fourth code segment using the results of the comparison operations to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the program determines that the gate has an acceptable noise immunity.

20. The computer-readable medium of claim 19, wherein the model generating code generates a fourth model of the gate, the fourth model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, the fourth ratio corresponding to a fourth numerical value, the fourth numerical value being used by the second code segment to access seventh and eighth threshold values stored in the memory device, wherein when the second input is low, the third code segment determines the noise level on the second input and wherein the fourth code segment compares the measured noise level to the seventh threshold value, and wherein when the second input is high, the third code segment determines the noise level on the second input and wherein the fourth code segment compares the measured noise level to the eighth threshold value, the fourth code segment using the results of the comparison to determine whether or not the gate meets acceptable noise immunity requirements with respect to the fourth model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first, second, third and fourth models, the program determines that the gate has an acceptable noise immunity.